IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A printed circuit board arrangement comprising:

a core substrate having a cavity;[[,]] and

a resin insulating layer and a conductor circuit laminated on the core substrate;[[,]]

a solder bump provided on the conductor circuit;

an IC chip having an electrode and mounted on an outer layer of the conductor circuit, the electrode of the IC chip facing and being connected to the [[via a]] solder bump located right under the IC chip; and

a plurality of capacitors accommodated in the cavity, the capacitors being located immediately below the IC chip.

2. (Previously Presented) A printed circuit board arrangement according to claim 1, wherein a resin is charged between the plurality of capacitors in the cavity, and the resin has a thermal expansion coefficient smaller than a thermal expansion coefficient of the core substrate.

3. (Previously Presented) A printed circuit board arrangement according to claim 1 or 2, wherein the resin layer has through holes.

4. (Previously Presented) A printed circuit board arrangement according to claim 1 or 2, wherein a metal film is formed on electrodes of the capacitor, and an electric connection for the electrodes formed with the metal film is established by plating.

5. (Previously Presented) A printed circuit board arrangement according to claim 4,

wherein the metal film formed on the electrodes of the chip capacitor is a plated film including copper as a main component.

6. (Previously Presented) A printed circuit board arrangement comprising:

a core substrate having a cavity therein, and

a resin insulating layer and a conductor circuit laminated on the core substrate, and

a plurality of capacitors accommodated in the cavity, wherein at least a part of electrodes of each capacitor is uncoated with a coating layer and exposed to the outside, and an electric connection for the electrode exposed from the coating layer is established by plating.

7. (Currently Amended/Withdrawn) A printed circuit board arrangement according to [[of]] claim 6, wherein each of the plurality of capacitors is a chip capacitor having electrodes formed along an inside of an outer edge thereof.

8. (Previously Presented/Withdrawn) A printed circuit board arrangement according to claim 6, wherein each of the plurality of capacitors is a chip capacitor having electrodes formed in matrix.

9. (Previously Presented/Withdrawn) A printed circuit board arrangement according to claim 6, wherein the plurality of capacitors are mounted on the surface of the printed circuit board.

10. - 78. (Canceled)